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PATENT, TRADEMARK, COPYRIGHT AND RELATED INTELLECTUAL PROPERTY LAW

March 22, 2006

Attn: The Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re:	U.S. Patent No.:	6,972,790 B2
	Issued:	December 6, 2005
	Title:	HOST INTERFACE FOR IMAGING ARRAYS
	Inventor:	Mark Suska
	Our Docket No.:	33214

Sir:

A Certificate of Correction under 35 U.S.C. 254 is hereby requested to correct Patent Office printing errors in the above-identified patent. Enclosed herewith is a proposed Certificate of Correction (Form No. PTO-1050) and documentation in support of the proposed corrections for consideration.

It is requested that the Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record.

Respectfully submitted,

By John P. Murtaugh
John P. Murtaugh, Reg. No. 34226

JPM/ck
Enclosures: Form PTO/SB/44

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

John P. Murtaugh
Name of Attorney for Applicant(s)

3-22-06 John P. Murtaugh
Date Signature of Attorney

PTO/SB/44 (07-03)
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,972,790 B2
DATED : December 6, 2005
INVENTOR(S) : Mark Suska

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 19

Line 2, after "claim", please delete "16" and insert therefor --15--.

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PATENT NO. 6,972,790 B2

No. of additional copies
⇨ 0

MAR 31 2006

Amendment filed 5/24/05

Re-numbered claim 15

16. (Currently amended) An integrated semiconductor imaging circuit ~~as claimed in claim 15 where the interface includes~~ for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- an interface integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system, the interface including:
  - a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
  - a circuit for controlling the transfer of the data from the memory to the data bus at a rate determined by the electronic processing system.

17. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes a first-in first-out (FIFO) buffer.

18. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.

19. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

Re-numbered claim 19

20. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes an addressable memory.